Part II

Chapter 5

Efficiency Optimization

This chapter is devoted to efficiency optimization within pulse modulation power amplifier systems. As introduced in Chapter 1 the fundamental goal of the present research is to develop amplifier solutions with significantly higher energy- and power-efficiency. A completely switched power stage has the inherent advantage of 100% efficiency in theory. Recall from chapter 4, that the efficiency will never reach this theoretical limit due to switch imperfections. In the present chapter, various contributions to efficiency degrading power loss will be analyzed theoretically. Starting with a simple switching leg, the results will be generalized to general PSC and Balanced PSC power stage topologies. Case examples are given to illustrate the efficiency and energy efficiency that can be achieved by the present state of technology within power switching devices and magnetics. The parametric dependencies and constraints in optimizing power stage efficiency will be discussed.

5.1 Efficiency in power conversion

It is bound with considerable difficulty to accurately model the power loss within power switching devices, given the existence of production spread and temperature variation in conduction and switching characteristics. One is often left with empirical tests and measurements in order to get exact results. However, reasonably accurate modeling of power loss within the PMA power stage is important, to allow optimization of system efficiency and energy efficiency. Various simplifications can make the estimation of power loss practical by relatively simple expressions. During the following investigations, the following simplifications will be made use of:

- Idealized switching characteristics, where current and voltage are assumed to have linear transition characteristics.
- The blanking time has been adjusted such as to avoid shoot-through phenomena.
- Diode reverse recovery is considered non-existent. The reverse recovery effect can contribute with significant switching losses, so the following analysis assumes that the effect is eliminated (e.g. by Schottky diodes as explained) or less significant.
- Several insignificant effects are omitted from the investigations, as the minimal contribution from diode conduction during the relatively short dead-band time.

Much progress in Power MOSFET technology has been made over the last decade. Thus, the recently introduced fifth generation provides an excellent combination of parameters. This continuous improvement of switches means that the PMA efficiency will converges towards the theoretical limit of 100% with time. Such improvements are not observed with existing linear amplification techniques that are stuck with power loss bound to the fundamental principles.

The analysis of power loss contributions will be divided into conduction losses and switching losses. A simple switching leg will be considered first, and following the results will be generalized to N switching legs in the general PSC and BPSC switching topologies. A terminology for the following analysis of current and conduction loss characteristics are defined below:

Parameter	Comment
I_L, $\hat{I}_L$, $I_{L,AV}$, $I_{L,RMS}$	Absolute, peak, average and RMS of *signal* (LF) current running to the load.
I_D, $\hat{I}_D$, $I_{D,AV}$, $I_{D,RMS}$	Absolute, peak, average and RMS of current in the switch.
I_T, $\hat{I}_T$, $I_{T,AV}$, $I_{T,RMS}$	Absolute, peak, average and RMS of the output HF ripple current component
I_{DT}, $\hat{I}_{DT}$, $I_{D,RMS}$	Absolute, peak and RMS of HF ripple current in the switch.
I_{LN}	Output current for each individual switching leg
L_N	Inductor required in each switching leg.
$M_{\max}$	Maximal modulation index
P_O, $P_{O,\max}$	Output power, maximal output power
V_O, $\hat{V}_O$, $\hat{V}_{O,\max}$	Output voltage, Peak output voltage and maximal peak output voltage.
I_O, $\hat{I}_O$	Absolute and peak output current
V_S	Power rail voltage
R_L	Load impedance
P_S, P_C, P_D, P_{TOT}, P_Q	Switching losses, conduction losses, total semiconductor losses, total output stage losses and quiescent losses.

5.2 Conduction losses

Fig. 5.1 illustrates currents I_L and I_D (high switch S_H) in a switching leg at various modulation depths, M=0, 0.3 and 0.8. The current during the positive going period is mainly delivered by the "high switch" S_H and vice versa. Observe how the output ripple current is minimal at maximal modulation depth.

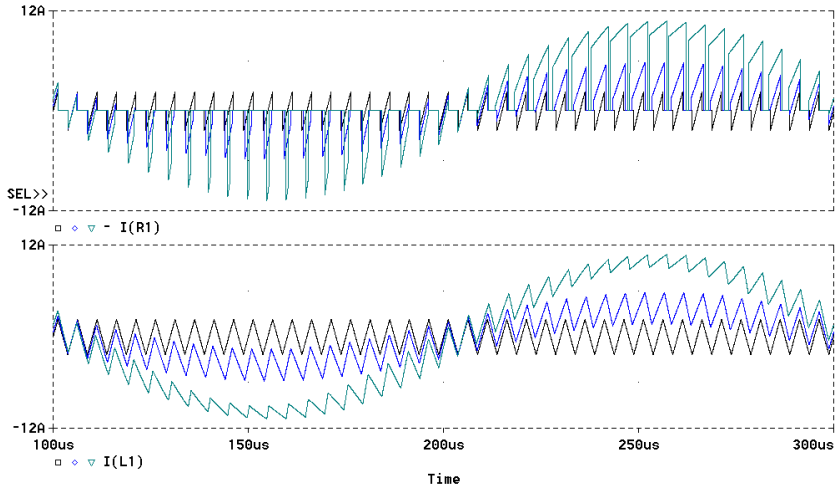


Fig. 5.1 Currents in a switching leg at three modulation depths, M = 0, 0.3, 0.8. Top – Current in "top" switch I_D. Bottom – output current = inductor current I_L.

The maximal required peak output voltage to deliver the desired power to the load is:

$$\hat{V}_{O,\max} = \sqrt{2R_L P_{O,\max}} \tag{5.1}$$

Limiting the modulation depth at $M_{\max}$ leads to the following necessary supply voltage V_S:

$$V_S = \frac{\hat{V}_O}{M_{\max}} \tag{5.2}$$

The peak output current is:

$$\hat{I}_O = \sqrt{\frac{2P_O}{R_L}} \tag{5.3}$$

It is assumed for simplicity that the signal current in the load and the output current are identical (i.e. no signal current in the filter capacitor), i.e.:

$$I_L = I_O \tag{5.4}$$

This assumption is valid as long as the frequency is well below the natural frequency of the demodulation filter. The rectified average and RMS values of the inductor current with sinusoidal modulation are:

$$I_{L,AV} = \frac{2}{\pi}\hat{I}_L \tag{5.5}$$

$$I_{L,RMS} = \frac{\hat{I}_L}{\sqrt{2}} \tag{5.6}$$

The load current is delivered from the two switches, and seen over a complete period of the modulating signal symmetry yields the same average and RMS currents in each switch. Subsequently the rectified average current and RMS current in the individual switch will be:

$$I_{D,AV} = \frac{1}{\pi}\hat{I}_L \tag{5.7}$$

$$I_{D,RMS} = \frac{\hat{I}_L}{2} \tag{5.8}$$

In the simple switching leg the ripple current magnitude is determined as:

$$\hat{I}_T = \frac{V_S}{2Lf_c} \tag{5.9}$$

This relation for $\hat{I}_T$ holds at zero modulation where the ripple current has maximal magnitude and contributes with maximal losses. However, it is assumed that $\hat{I}_T = \hat{I}_{T,\max}$ throughout the following to simplify the investigations. Furthermore, the switching voltage over the inductor is assumed to be $2V_s$ in (5.9), corresponding to a perfectly demodulated output. This simplification only marginally influences the investigations of the ripple current effects. The RMS value of the triangular ripple current is:

$$I_{T,RMS} = \frac{\hat{I}_T}{\sqrt{3}} \tag{5.10}$$

The symmetrical distribution of currents in the two switches within a complete switching cycle yields the following RMS ripple current is each switch:

$$I_{DT,RMS} = \frac{\hat{I}_T}{\sqrt{6}} \tag{5.11}$$

All essential currents have now been determined for the investigations of conduction loss within the switching leg. The semiconductor conduction loss for the switching leg is simply the sum of the two contributions:

$$\begin{aligned} P_C(I_L) &= 2R_{DS(on)}(I_{D,RMS}^2 + I_{T,RMS}^2) \\ &= 2R_{DS(on)}\left(\frac{\hat{I}_L^2}{4} + \frac{1}{12}\left(\frac{V_S}{Lf_c}\right)^2\right) \end{aligned} \tag{5.12}$$

The second contribution will generally only be of significance at quiescence. It should be emphasized, that $R_{DS(on)}$ depend strongly on the junction temperature. It is very important to consider this dependency for a reasonable estimate of conduction losses.

5.3 Switching losses

As illustrated in Chapter 4 the switching transitions for both current and voltage have a finite duration. During current or voltage switching, the switching device is in the active region leading to switching losses. The non-linear switching characteristics and multi-parameter dependency of several physical parameters makes it difficult to perform a generalized analysis. However, by simplifying the switching characteristics as shown in Fig. 5.2, the analysis can be much simplified. The scenario is repeated in every switching cycle with a positive load current. Since the switching losses are an *even* function of the load current (symmetry), only the situation with positive load currents will be considered.

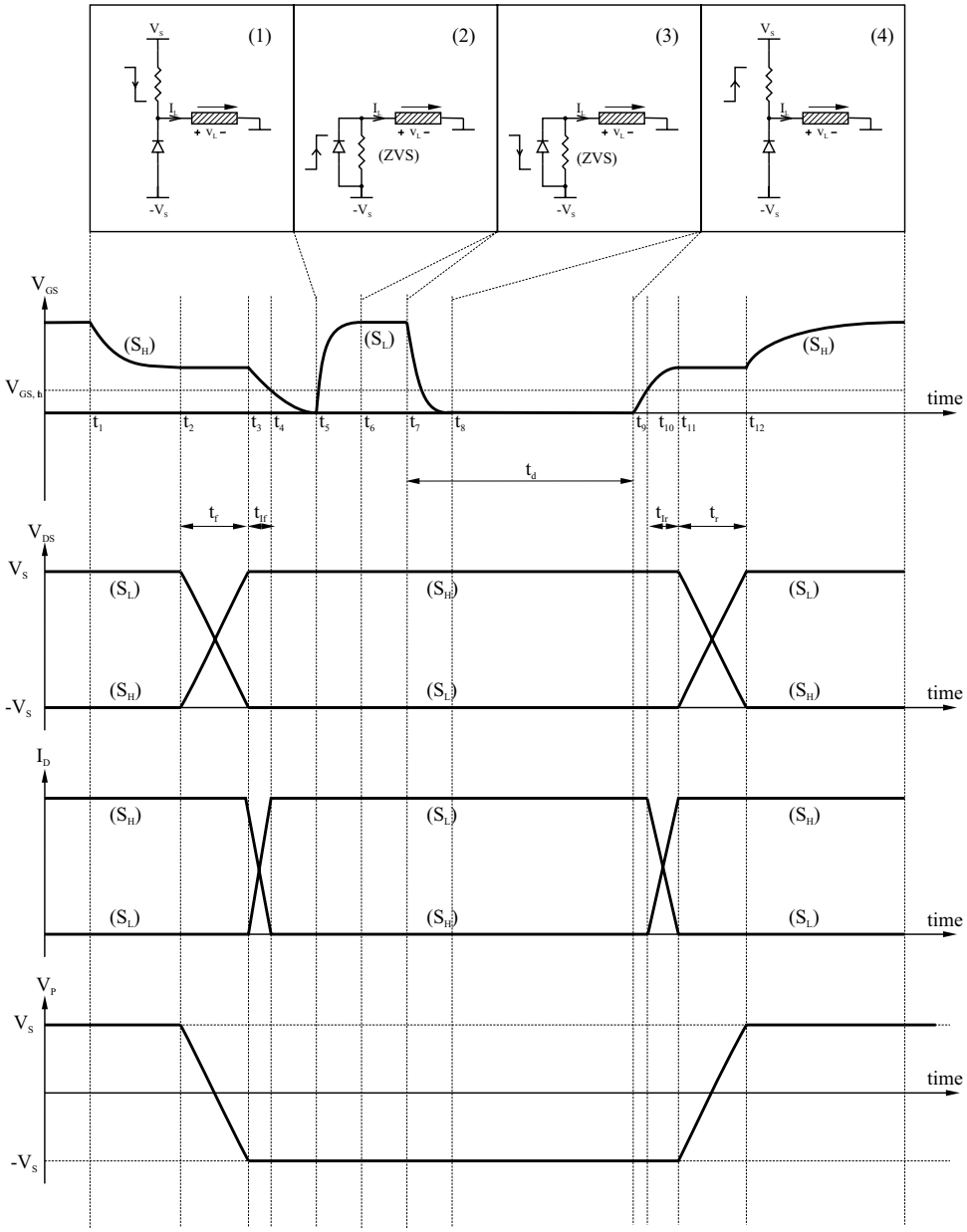


Fig. 5.2 Simplified switching characteristics for estimation of switching losses.

At lower currents where $\hat{I}_L < \hat{I}_T$, *all* switching actions will be ZVS and there will be no contributions from switches that enter the active region. For $\hat{I}_L > \hat{I}_T$, a switching cycle involves the following actions in the switching leg:

- One full turn-on.
- One full turn-off.
- One ZVS turn-on.
- One ZVS turn-off.

ZVS transitions produce negligible losses in the switching transistors. With the linear approximation, the contributions from the full turn-on and full turn-off can be derived from simple geometric relations. From Fig. 5.2, the following energy loss is introduced the falling transition $t_2 - t_4$:

$$E_{S,fall}(I_L) = \frac{1}{2} 2 V_S I_L (t_f + t_{If}) \tag{5.13}$$

Note that the switching voltage over the individual devices is $2V_S$. The voltage fall and current fall times are:

$$t_f = \frac{Q_{GD}}{\frac{v_{GS,th} + \frac{I_L}{g_{fs}}}{R_G}} \tag{5.14}$$

$$t_{If} = R_G C_{iss} \ln\left(\frac{v_{GS,th} + \frac{I_L}{g_{fs}}}{v_{GS,th}}\right) \tag{5.15}$$

Similarly, the energy loss from the rising voltage and current transition $t_9 - t_{12}$ is given by:

$$E_{S,rise}(I_L) = \frac{1}{2} 2 V_S I_L (t_r + t_{Ir}) \tag{5.16}$$

Where:

$$t_r = \frac{Q_{GD}}{\frac{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}}{R_G}} \tag{5.17}$$

$$t_{Ir} = R_G C_{iss} \ln\left(\frac{V_G - v_{GS,th}}{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}}\right) \tag{5.18}$$

By averaging over a complete period of the signal, the total switching losses arising from voltage and current transitions of finite duration are:

$$P_{S1}(I_L) = \begin{cases} 0 & (\hat{I}_L < \hat{I}_T) \\ \frac{1}{2} f_c 2V_S \frac{\hat{I}_L}{\pi}(t_f + t_{If} + t_r + t_{Ir}) & (\hat{I}_T < \hat{I}_L) \end{cases} \tag{5.19}$$

In practice, the transition between states is not as sharp as indicated. Some current is necessary to provide the ZVS transition, i.e. $\hat{I}_L$ has to be somewhat lower than $\hat{I}_T$ for a full ZVS transition. A further contribution to switching losses arises from the parasitic output capacitance of the switches that are charged and discharged within each period.

$$P_{S2} = (2V_S)^2 C_{DS} f_c = 4C_{DS} f_c V_S^2 \tag{5.20}$$

The voltage dependency of C_{DS} has to be considered. A conservative but reasonable estimate of the losses can be made by using the output capacitance at 10-20% of the breakdown voltage. Each switch contributes with losses due to their output capacitance. Consequently, the total switching losses in the switching can be approximated by:

$$\begin{aligned} P_S(I_L) &= P_{S1}(I_L) + 2P_{S2} \\ &= \begin{cases} 8C_{DS} f_c V_S^2 & (\hat{I}_L < \hat{I}_T) \\ f_c V_S \frac{\hat{I}_L}{\pi} \tau(I_L) + 8C_{DS} f_c V_S^2 & (\hat{I}_T < \hat{I}_L) \end{cases} \end{aligned} \tag{5.21}$$

Where:

$$\tau(I_L) = R_G Q_{GD} \left(\frac{1}{v_{GS,th} + \frac{I_L}{g_{fs}}} + \frac{1}{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}} \right) + R_G C_{iss} \ln \left[\frac{v_{GS,th} + \frac{I_L}{g_{fs}}}{v_{GS,th}} \cdot \frac{V_G - v_{GS,th}}{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}} \right] \tag{5.22}$$

The total power loss in the switching leg is the sum of conduction loss (5.12) and the total switching losses (5.21).

5.4 Demodulation filter losses

Filter inductors generally adds another significant contribution to the total power loss in PMA systems. This contribution is generally comparable to that of the switching power stage and it is important to obtain a reasonable accurate estimate of the losses. The following elements contribute to the power loss within the filter inductor(s):

- Conduction losses caused by LF current running in the finite DC resistance of the inductor.
- Conduction losses caused by the HF ripple current running in the inductor.
- Magnitic core losses due to LF induction swing
- Magnetic core losses caused by the ripple current (a HF induction swing).

It is impossible to generalize about the significance of each contribution. The typical characteristics will be illustrated by considering a specific type of inductor. Generally, single layered toroids are a good solution, that provides the highest resonance frequency, minimal volume and also a very high efficiency, by carefull design and proper selection of magnetics. Subsequently, the investigations will focus on torodial inductors. A set of parameters for the analysis are defined below.

Parameter	Description
N_L	Number of turns
A_L	Permeance (H)
B , $\hat{B}$, $\hat{B}_{\max}$	Induction, peak induction and maximal peak induction (T)
Φ	Magnetic flux (Wb)
$\varnothing_{cu}, l_{cu}, R_{cu}$	Winding parameters (diameter, length, resistance)
ρ_{cu}	Specific resistance of copper ($0.0155\Omega mm^2/m$)
μ_0 , μ_r	Vacuum permeability (H/m), relative permeability.
d_i , d_O , h	Inner and outer diameter and height of magnetic core
A_T , l_T , V_T	Cross-sectional area, middle-length and volume of core.
P , B_r , f_r , k_f k_B	Core loss parameters
P_{cu}	Copper loss (inductor conduction loss)
P_{co}	Core loss
P_F	Total filter losses

For torodial inductors with a distributed airgab the necessary number of turns to realize a given inductance is:

$$N_L = \sqrt{\frac{L}{A_L}} \tag{5.23}$$

Where the permeance is defined as:

$$A_L = A_T \frac{\mu_0 \mu_r}{l_T} \tag{5.24}$$

By combining Amperes law:

$$N_L I_L = \frac{B l_T}{\mu_0 \mu_r} \tag{5.25}$$

And the general definition of inductance:

$$L = \frac{N \Phi}{I_L} \tag{5.26}$$

The following central relation for filter inductor design arrives:

$$B = \frac{L I_L}{A_T N_L} \tag{5.27}$$

The relation dictates the maximal allowable inductor peak current for linear operation:

$$\hat{I}_{L,\max} \leq \frac{\hat{B}_{\max} A_T N_L}{L} \tag{5.28}$$

5.4.1 Conduction losses

Conduction losses are introduced due to the finite DC impedance of any inductor. The DC impedance of the winding on a single layer toroidial inductor is:

$$R_{cu} = \frac{N_L l_V \rho_{cu}}{\left(\frac{\varnothing_{cu}}{2}\right)^2 \pi} \tag{5.29}$$

Where the average winding length is:

$$l_V = 2h + (d_O - d_I) + 4\varnothing_{cu} \tag{5.30}$$

For a single layer winding the maximal winding diameter is:

$$\varnothing_{cu,\max} = \frac{d_I \pi}{N_L} \tag{5.31}$$

The resulting conduction losses will be a superposition of the two contributions:

$$P_{cu}(I_L) = R_{cu}(I_{L,RMS}^2 + I_{T,RMS}^2) \tag{5.32}$$

5.4.2 Core losses

Due to the magnetic hysteresis power dissipation within the core material will exist. By a reasonable choice of core material, core losses are only significant in the idle situation. The core losses can be expressed as the sum of the two contributions:

$$P_{co}(I_L) = PV_T \left[\left(\frac{f_B}{f_r} \right)^{k_f} \left(\frac{B(I_L)}{B_r} \right)^{k_B} + \left(\frac{f_c}{f_r} \right)^{k_f} \left(\frac{B(I_T)}{B_r} \right)^{k_B} \right] \tag{5.33}$$

The simple expression is based on the assumption that the HF current is a sinusoidal current with amplitude $\hat{I}_T$ and frequency f_c. This is a valid assumption, since higher frequency components have considerably lower amplitude. The HF contribution can be made negligible by a suitable choice of core material. In (5.33) it is furthermore assumed that the HF induction swing is *constant* although the average induction swing is lower at high output levels. The resulting filter losses for the switching leg is the sum of the conduction loss and core loss:

$$P_F(I_L) = P_{cu}(I_L) + P_{co}(I_L) \tag{5.34}$$

5.5 Generalization to BPSC and PSC

The PSC switching power stage topology is realized by N parallel coupled switching legs. In the balanced configuration for the BPSC topology, there are N/2 parallel-coupled switching legs driving each end of the load. Correspondingly, the output current for each individual switching leg, I_{LN}, is related to the total output current I_O as:

Switching leg	PSC	BPSC
$I_{LN} = I_O$	$I_{LN} = I_O / N$	$I_{LN} = 2I_O / N$

Due to the paralleling of switching legs and balanced drive in BPSC, the required inductance in each individual switching leg, L_N, is dependent upon the number of switching legs. The paralleling of N switching legs in PSC corresponds to a paralleling of N inductors. Similarly, the balanced drive in BPSC corresponds to a series coupling of two sets of N/2 inductors. Correspondingly, the inductor L_N required for each switching leg for the general PSC and BPSC switching topologies are:

Switching leg	PSC	BPSC
$L_N = L$	$L_N = L \cdot N$	$L_N = L \cdot N / 4$

The voltage swing over the inductors, corresponding to the necessary breakdown voltage depends on power stage topology as:

Switching leg	PSC	BPSC
$2V_S$	$2V_S$	V_S

With these definitions, the general expressions for *total* semiconductor loss and filter loss in an N-leg PSC or BPSC output stage is:

$$P_D(I_O) = N \cdot [P_S(I_{LN}) + P_C(I_{LN})] \tag{5.35}$$

$$P_F(I_O) = N \cdot [P_{cu}(I_{LN}) + P_{co}(I_{LN})] \tag{5.36}$$

These expressions are general with the relationships that have been established between I_O and I_{LN} above.

5.6 Case example

A case example is considered to illustrate the efficiency level that can be achieved by a switching power stage, using the present state of technology. The synthesis of a 200W power stage is considered. The general parameters are summarized below:

Parameter	Description
$P_{O,\max}$	200W
R_L	4Ω
f_B	20KHz
f_O	$2f_B$
Q_O	$\frac{1}{\sqrt{3}}$
V_S	44V ($M_{\max}$ =0.9)

f_B, f_O and Q_O represent the PMA target bandwidth, the filter natural frequency and the filter Q, respectively. The optimization is carried output using the Power Stage Optimization Tool (PSOT) that has been developed to automate PSC and BPSC power stage design. The MATLAB toolbox is described more closely at the end of this chapter. The following topologies will be optimized for this specific application:

- PSC with N=1. (i.e. a simple switching leg).
- BPSC with N=2. (i.e. a H-bridge).
- BPSC with N=4.

The power stages will be implemented with realistic switching devices and filter core materials. Throughout the investigations, it will be assumed that the junction temperature is 120°. This causes the ON impedance to be 50-60% higher than the nominal value.

5.6.1 Implementation with a simple switching leg

In this simplest possible realization the voltage requirements for the two switches is $2V_S$=88V. The power stage implementation is investigated using 100V MOSFET technology although the derating factor is low. An appropriate switch for the application is a 50mΩ/100V MOSFET type. The gate driver parameters are set at (V_G=12V, R_G=5Ω) as a compromise between losses and noise. The filter core material is low μ_r iron power with good HF characteristics. Fig. 5.3 shows the distribution and total semiconductor losses vs. output power and Fig. 5.4 shows the efficiency of the switching leg, filter and the total system efficiency. The results are summarized below.

Parameter	Description
f_c	300KHz
L_N	27 μH
$\hat{I}_{LN} = \hat{I}_O$	10A
P_Q	1W
$P_{TOT,\max}$	13.5W
Efficiency	93.5%
Energy efficiency	32%

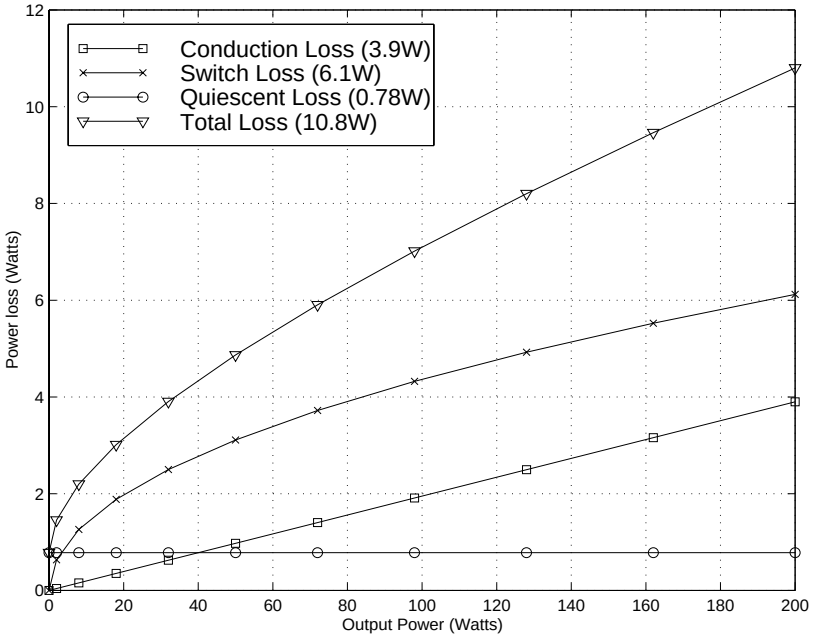


Fig. 5.3 Semiconductor losses in a switching leg implementation of the case example.

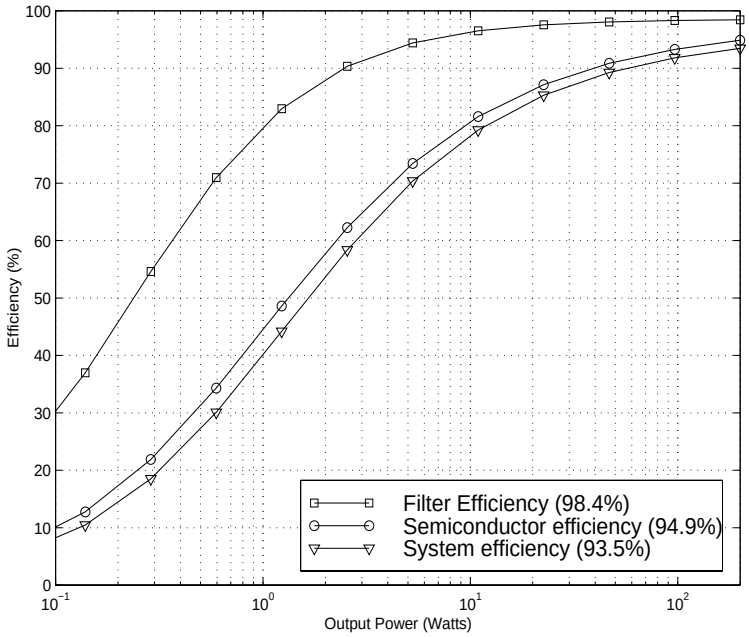


Fig. 5.4 Efficiency of the switching power stage, the filter and complete system in a switching leg realization of the power stage case example.

The energy efficiency is calculated directly from the system power dissipation as defined in chapter 1 with the specified time distribution of relative output levels. The average output power from the amplifier is thus $P_{O,AV} = 350mW$ under the given assumptions (Table 1.1), whereas the average power dissipation over time is calculated to $P_{TOT,AV} = 1.1W$. Clearly, the given realization provides a dramatic improvement in energy efficiency of more that an order of magnitude compared to conventional amplifier principles. The main reason is the optimization towards minimal power loss of only 1W at quiescence. It should be remembered however, that the losses of the other elements as driver circuitry are not included.

5.6.2 BPSC realization (N=2)

The BPSC topology with N=*2* corresponds to the conventional H-bridge. The four switches all handle the same current as the switching leg for a given output, i.e. the conduction losses will inevitably increase. However, rich compensation is provided by the reduced voltage requirements for each individual switch, which is halved to $V_S = 44V$. For comparison with the switching leg, the losses in the bridge configuration have been investigated with the same parameters (i.e. components) as above. Fig. 5.5 shows the semiconductor losses in each of the two switching legs. Whereas the conduction losses in each leg are unchanged, the switching losses are approximately reduced by 50% in each leg. With four switches the switching losses remain *unchanged* whereas the conduction loss *doubles* causing the total efficiency to reduce to 91.7%. However, the lower voltage requirement means that 60V technology becomes a feasible alternative. The efficiency can be improved by a better compromise between ON-resistance and parasitic capacitance, e.g. a 25mΩ/60V. This will lead to system efficiency above 93% as for the simple switching leg. The efficiency of the four-transistor output stage configuration closely resembles what is achieved above by the switching leg.

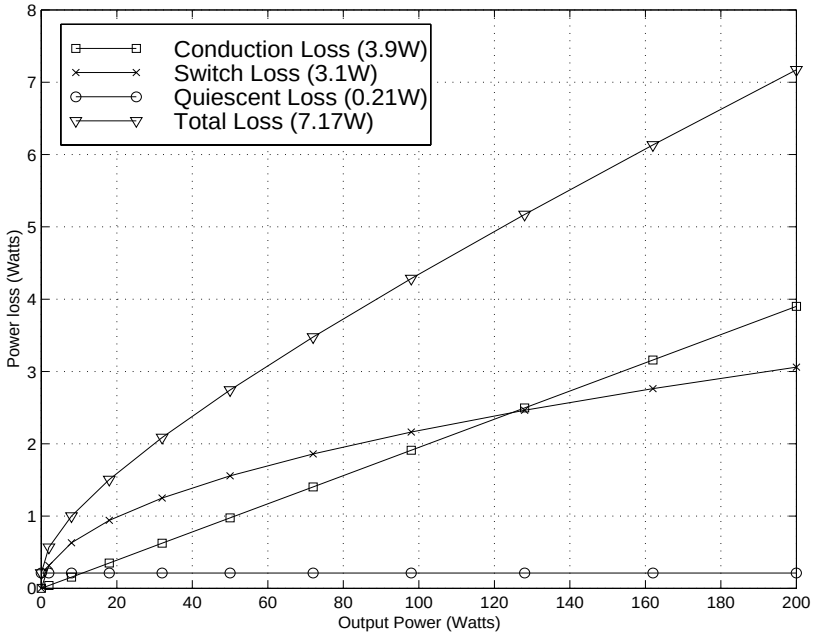


Fig. 5.5 Semiconductor losses in each of the two switching legs for the BPSC (N=2) implementation of the case example.

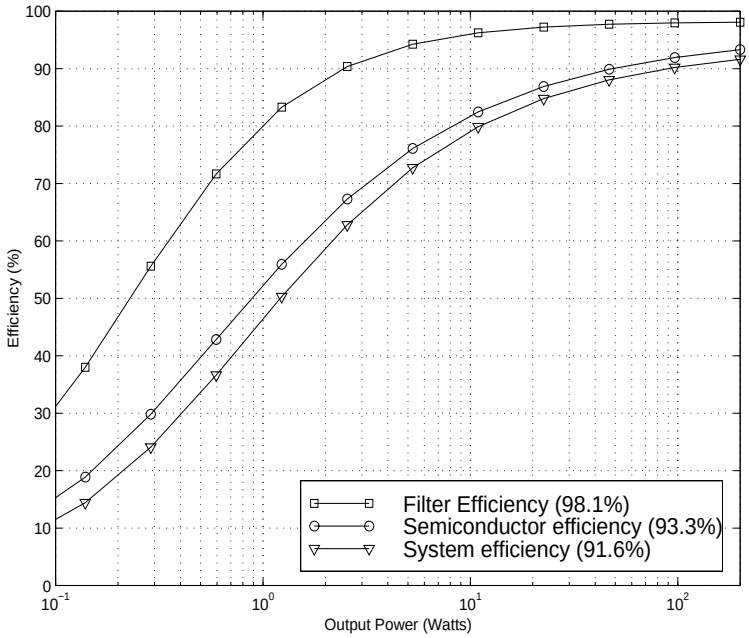


Fig. 5.6 Efficiency of the BPSC (N=2) realization of the case example PMA.

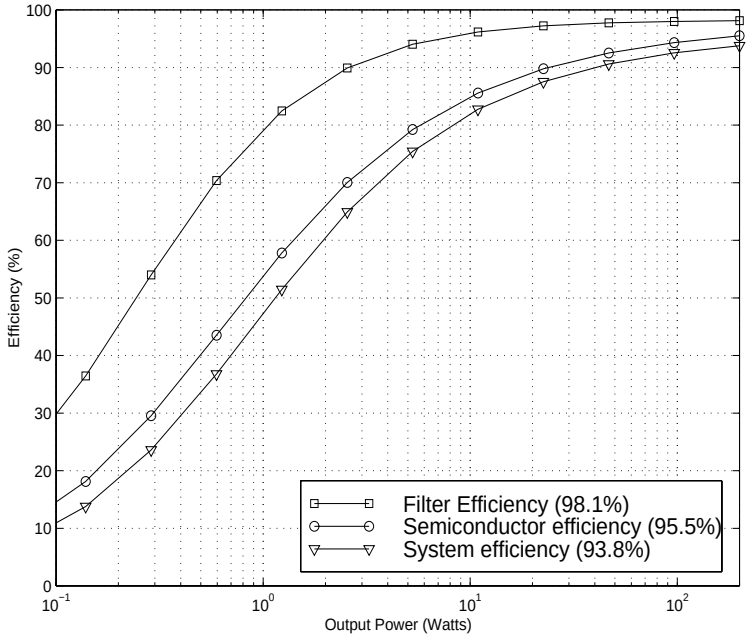


Fig. 5.7 Efficiency of the BPSC (N=2) realization of the PMA case example with optimized 60V switches.

Parameter	Description
f_c	300KHz
L_N	13.5 μH
$\hat{I}_{LN,\max} = \hat{I}_{O,\max}$	10A
P_Q	0.8W
$P_{TOT,\max}$	13.1W
Efficiency	93.6%
Energy efficiency	40%

The improvement in energy efficiency is caused by the reduced switching voltage for the parasitic output capacitance of the switches. Halving the voltage reduces the individual contributions by a factor of four in each switch.

5.6.3 BPSC realization (N=4)

The BPSC topology with *N=4* significantly changes the power loss in the individual switching legs. The peak current in each switching leg and filter inductor is *halved*, compared to both the simple switching leg and the bridge considered previously. The voltage requirement for each switch is 44V with the given specifications, independent upon N. This renders the use of 60V possible and the application of a 25mΩ/60V switch is considered.

Another essential issue of BPSC power stage optimization is the carrier frequency, which can be reduced as a consequence of the improved synthesis of the modulating signal. The carrier frequency throughout this case example is halved to 150KHz, corresponding to an effective sampling frequency of 600KHz. Fig. 5.8 shows the semiconductor losses in each of the four switching legs. Looking at the individual switching leg, switching losses are *halved* and conduction losses reduced by a *factor of four* compared with the single leg realization. The maximal power dissipation of each switch barely 600mW at the maximal output power of 200W (!). Fig. 5.9 shows the system efficiency vs. output power. Clearly, PSCPWM provides improved efficiency at higher output levels. The efficiency of 96% is extremely high for a full bandwidth, high power PMA. Essential parameters for The BPSC realization of the 200W power stage are summarized below.

Parameter	Description
f_c	150KHz
L_N	27 μH
$\hat{I}_{LN,\max} = \hat{I}_{O,\max}/2$	5A
P_Q	1.1W
$P_{TOT,\max}$	8.3W
Efficiency	96%
Energy efficiency	32%

It is important to emphasize a fundamental property of PSCPWM. Under the assumption that the switch and inductor resistance to not change with N the conduction losses in both filter and switching power stage will be *inversely proportional to N*.

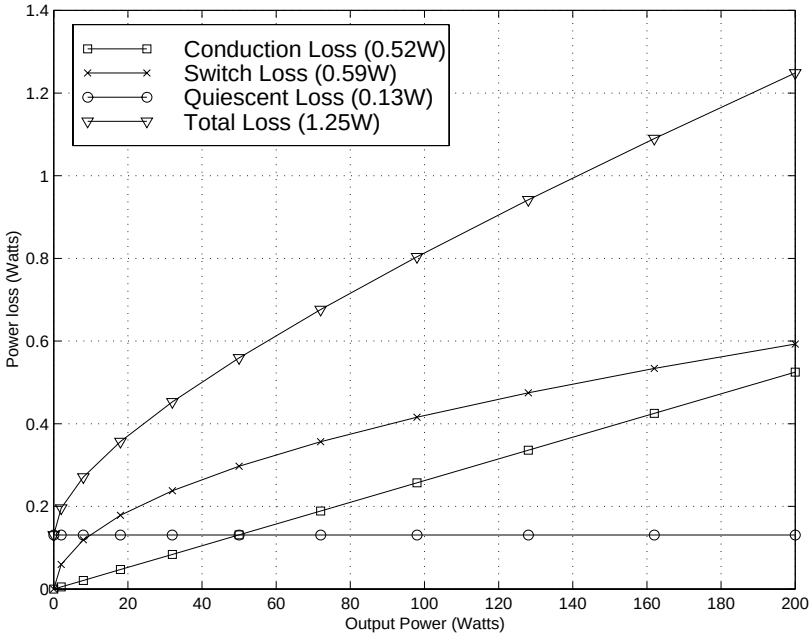


Fig. 5.8 Semiconductor loss in a single switching leg with a BPSC realization (N=4).

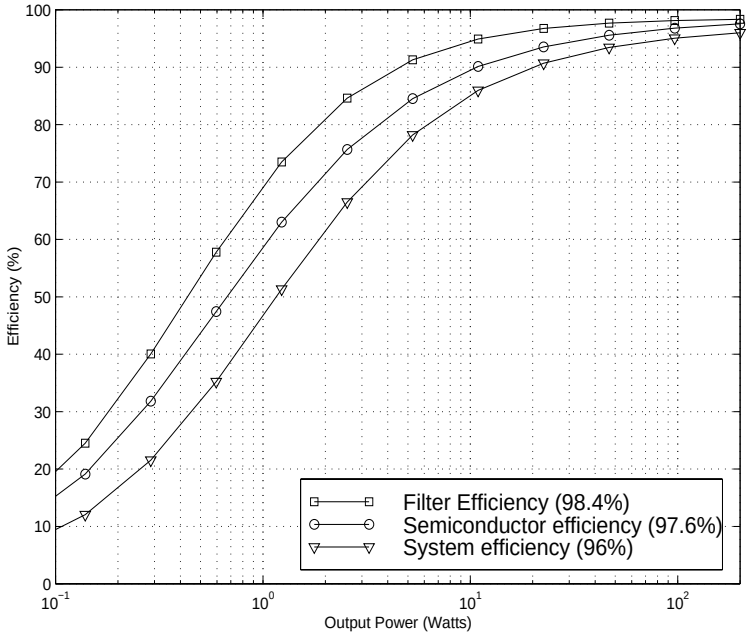


Fig. 5.9 System efficiency in a BPSC realization *(N=4)*. The excellent efficiency is achieved by a low carrier frequency minimizing switching losses and the reduced conduction losses achieved by dividing current.

5.6.4 BPSC in high power realizations

Balanced PSCPWM realized with the BPSC power stage has shown to provide both improved modulation and higher efficiency. The true potential of PSCPWM becomes apparent in higher power systems, where it gets problematic or even impossible to implement the power conversion stage with a bridge or a switching leg. PSCPWM is a very elegant solution in this case. This will be demonstrated by considering an 800W power stage, suitable for e.g. general-purpose professional power amplification. Besides the wider power range, the fundamental parameters from above are left unchanged. With $N = 4$ the following is achieved with the BPSC 800W power stage:

Parameter	Description
V_S	88V
f_c	150KHz
L_N	$27\,\mu H$
$\hat{I}_{LN,\max}$	10A
P_Q	4W
$P_{TOT,\max}$	43W
Efficiency	95%
Energy efficiency	35%

Fig. 5.10 shows the power loss in a single switching leg with 50mΩ/100V MOSFET technology. The stress of each individual switching leg is minimal.

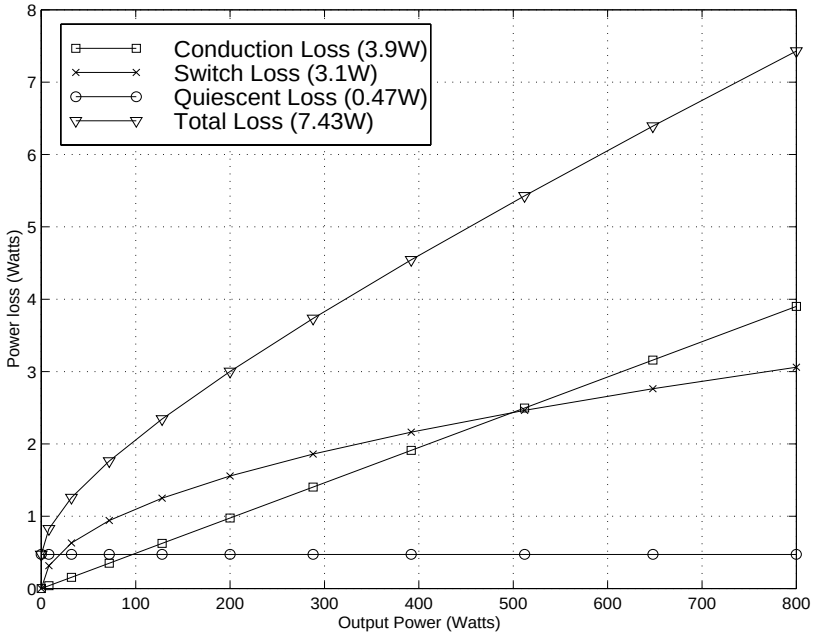


Fig. 5.10 Semiconductor loss in one of the switching legs in a 800W BPSC (N=4) case example. The stress of each individual switching leg is minimal even at full load.

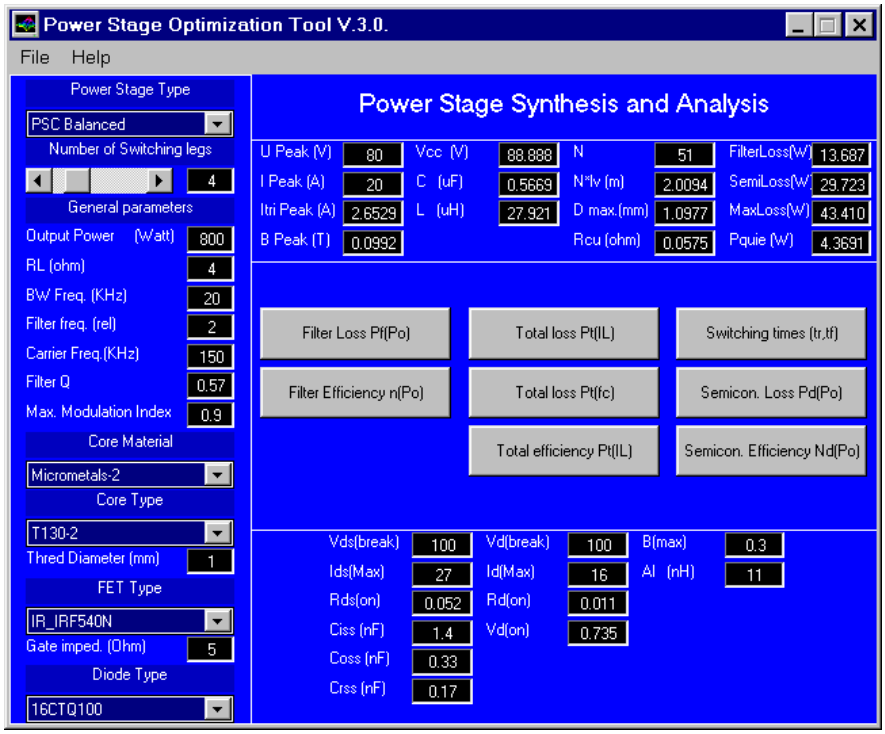
5.7 Summary

This chapter was devoted to efficiency optimization in the switching power stage of PMA systems. The contributions to power dissipation within output stages has been investigated and general analytical expression for power dissipation in PSC and BPSC switching power stages have been derived. The increasing number of power components in the general PSC and BPSC topologies was shown not to compromise efficiency. On the contrary, improvements in efficiency are generally possible. It is important to emphasize a fundamental property of PSCPWM. Under the assumption that the parasitic MOSFET and inductor resistance does not change with N, the conduction losses in both filter and switching power stage will be *inversely proportional to N*. Furthermore, switching losses are reduced as a consequence of the lower switching frequency and lower current in each switching leg.

Case examples has been investigated, showing the excellent efficiency and energy efficiency that can be achieved by the present state of technology within the field of power switching devices and magnetics. To conclude, in practical PMA applications within the range of a few hundred watts of output power, the heat sink will virtually be eliminated. Furthermore, the energy efficiency can be improved by an order of magnitude.

5.7.1 PSOT – A MATLAB toolbox for power stage optimization

Power stage optimization is a tedious process since the various loss contributions depend on a range of parameters. A power stage optimization toolbox has been developed for MATLAB [Ch98], [Fr98] for swift and automated power stage synthesis of the general PSC and BPSC topologies. The toolbox is GUI controlled with push button access to all essential functions. The GUI is shown below.



The “snap-shot” corresponds to the 800W BPSC realization that was considered in the chapter. Controllable parameters on the GUI are:

- Topology (PSC, BPSC)
- Number of switching legs
- General parameters as Output power, Load impedance, ...
- Core material (selected from a library)
- MOSFET (selected from a library)

Based on these input specifications the output panels provide all interesting parameters. The push buttons provides access to various parametric investigations of power stage loss and efficiency.